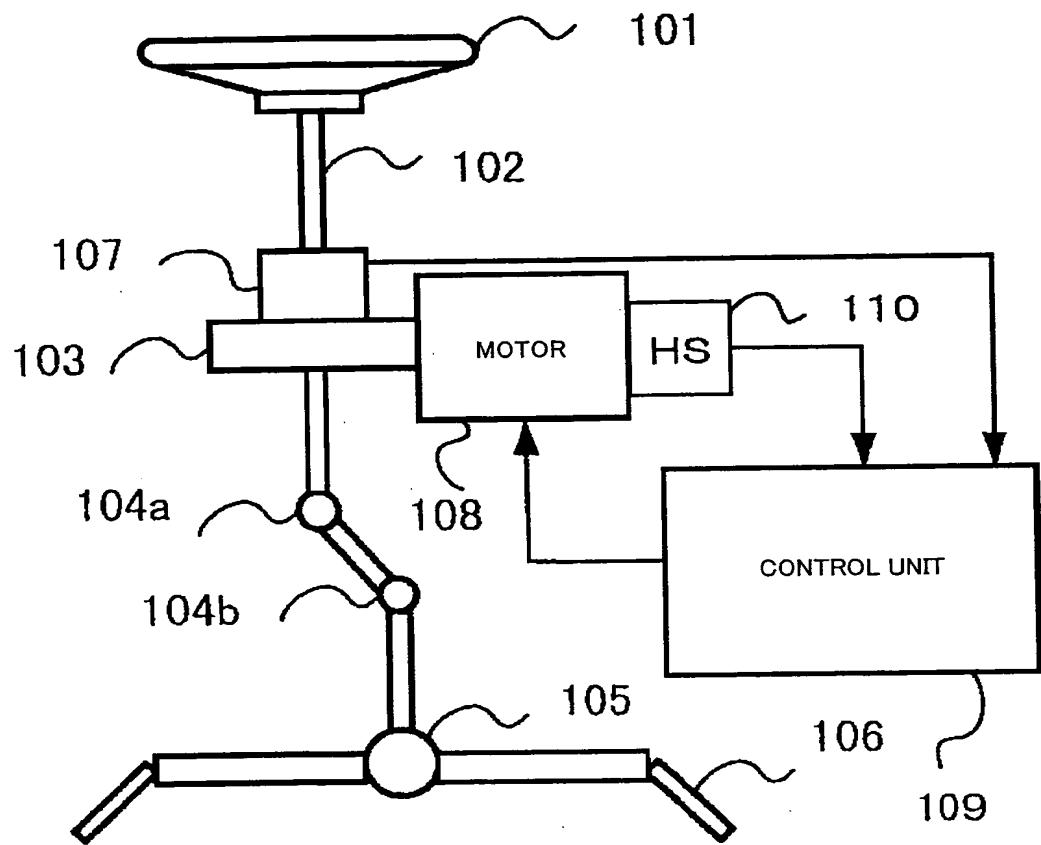


FIG.1



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FIG.2

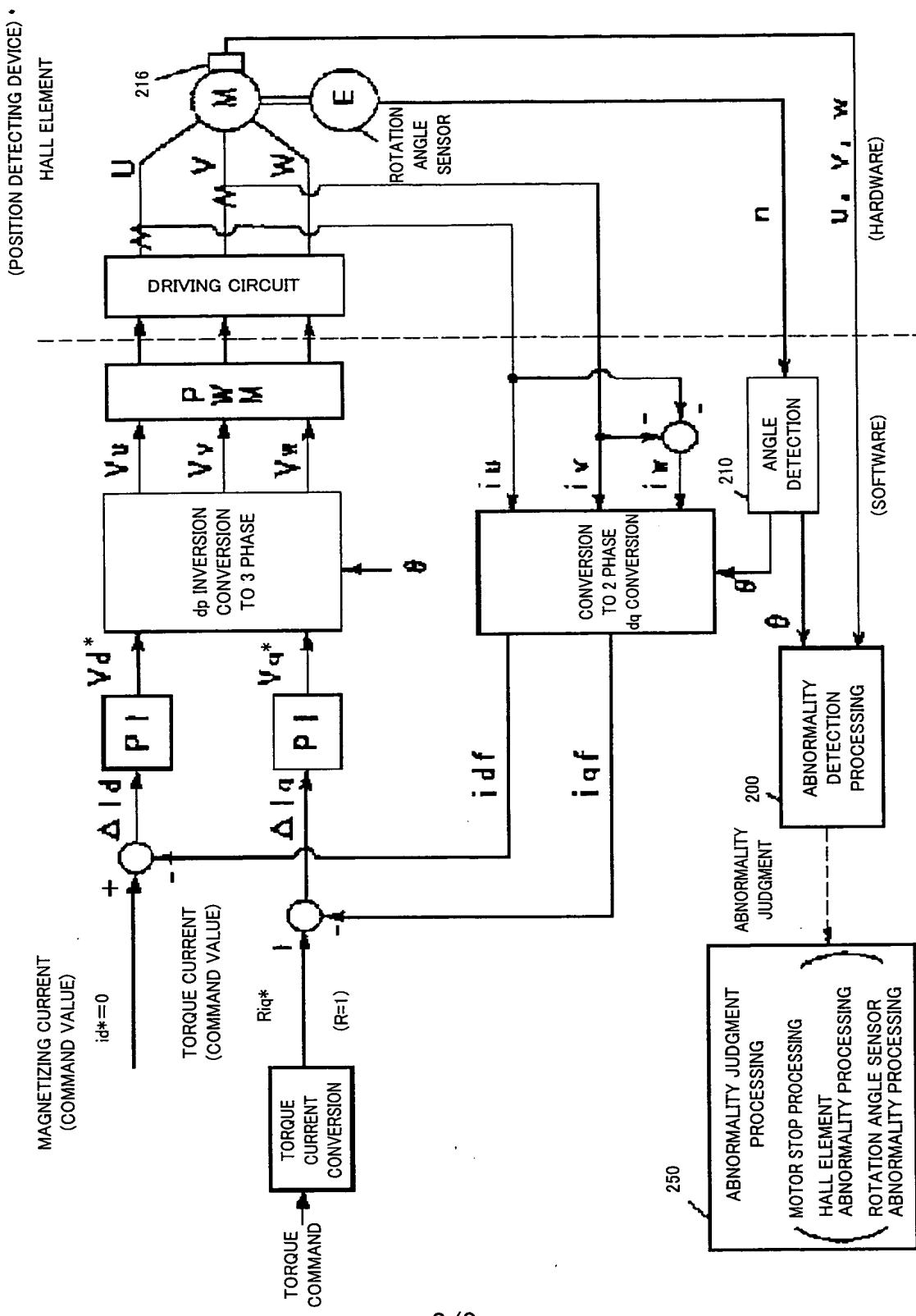


FIG.3

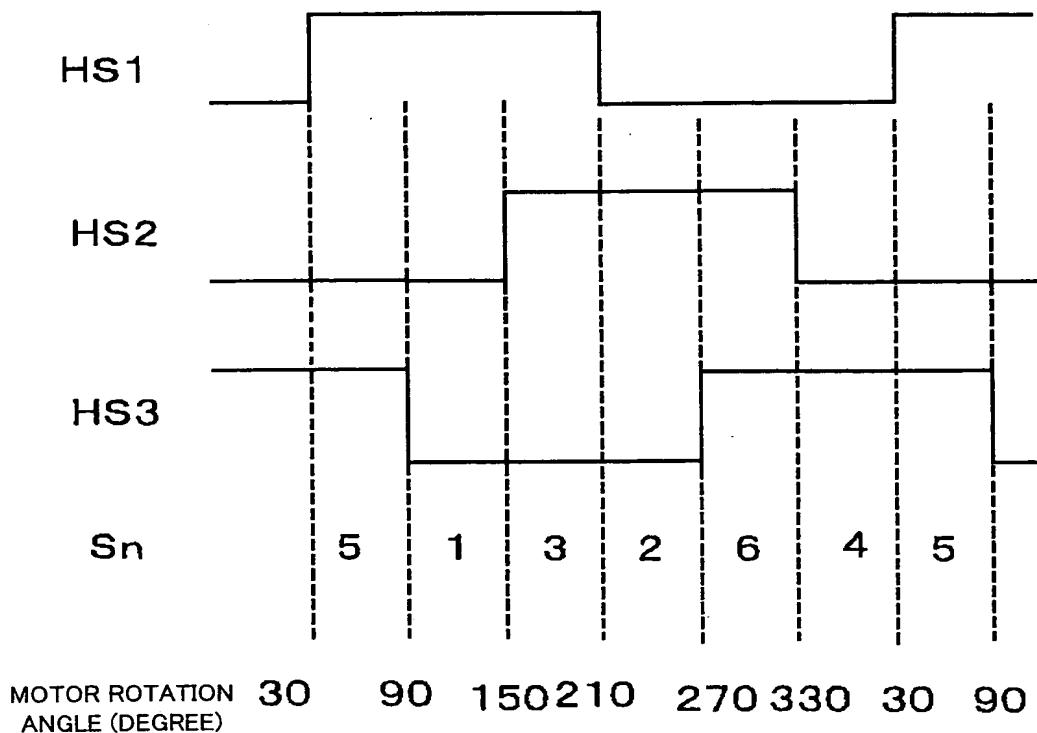


FIG.4

HS3 (bit 2)	HS2 (bit 1)	HS1 (bit 0)	S
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FIG.5

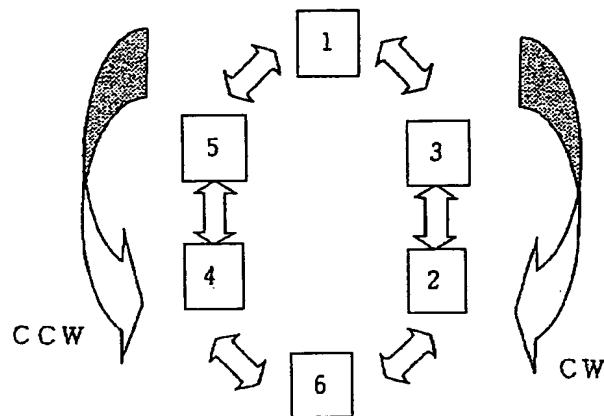


FIG.6

S_n S_{n-1}	1	2	3	4	5	6
1	0	E	CW	E	CCW	E
2	E	0	CCW	E	E	CW
3	CCW	CW	0	E	E	E
4	E	E	E	0	CW	CCW
5	CW	E	E	CCW	0	E
6	E	CCW	E	CW	E	0

FIG.7

S_n S_{n-1}	0	1	2	3	4	5	6	7
0	E	E	E	E	E	E	E	E
1	E	0	E	CW	E	CCW	E	E
2	E	E	0	CCW	E	E	CW	E
3	E	CCW	CW	0	E	E	E	E
4	E	E	E	E	0	CW	CCW	E
5	E	CW	E	E	CCW	0	E	E
6	E	E	CCW	E	CW	E	0	E
7	E	E	E	E	E	E	E	E

FIG.8

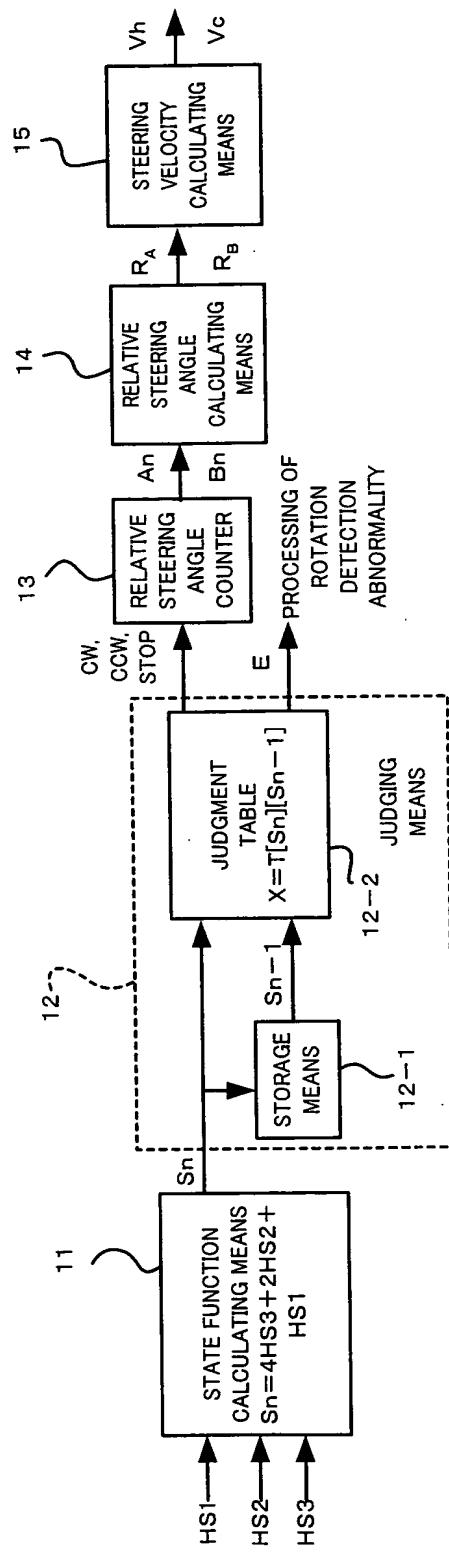


FIG.9

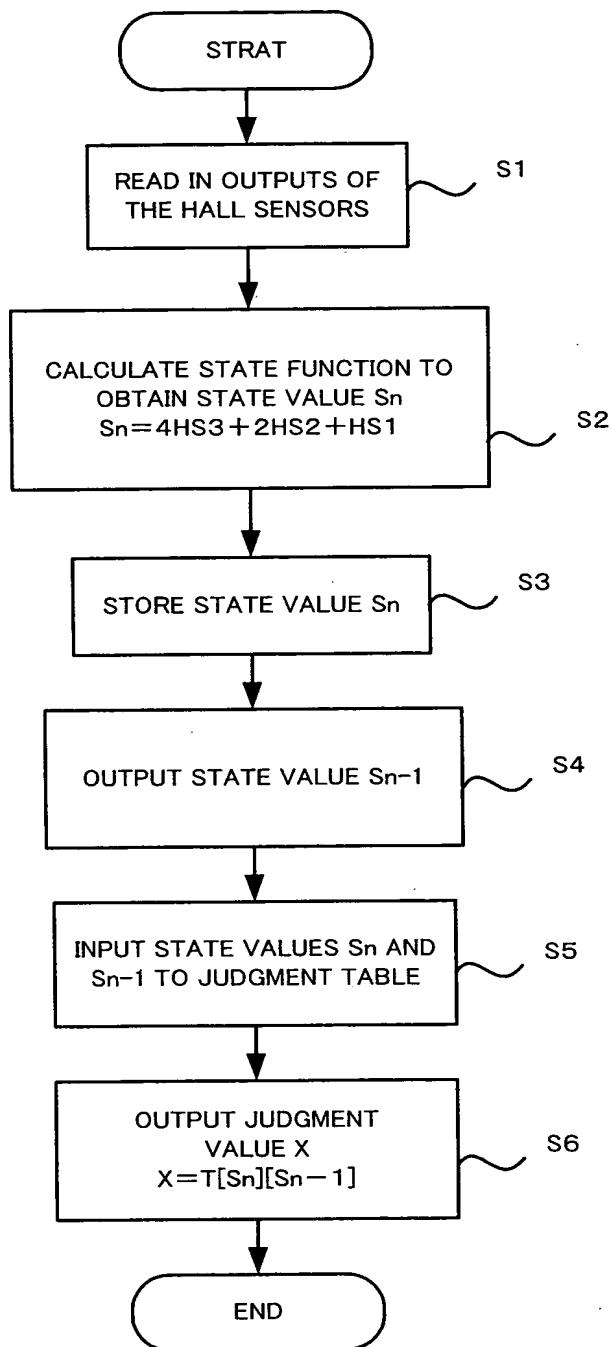
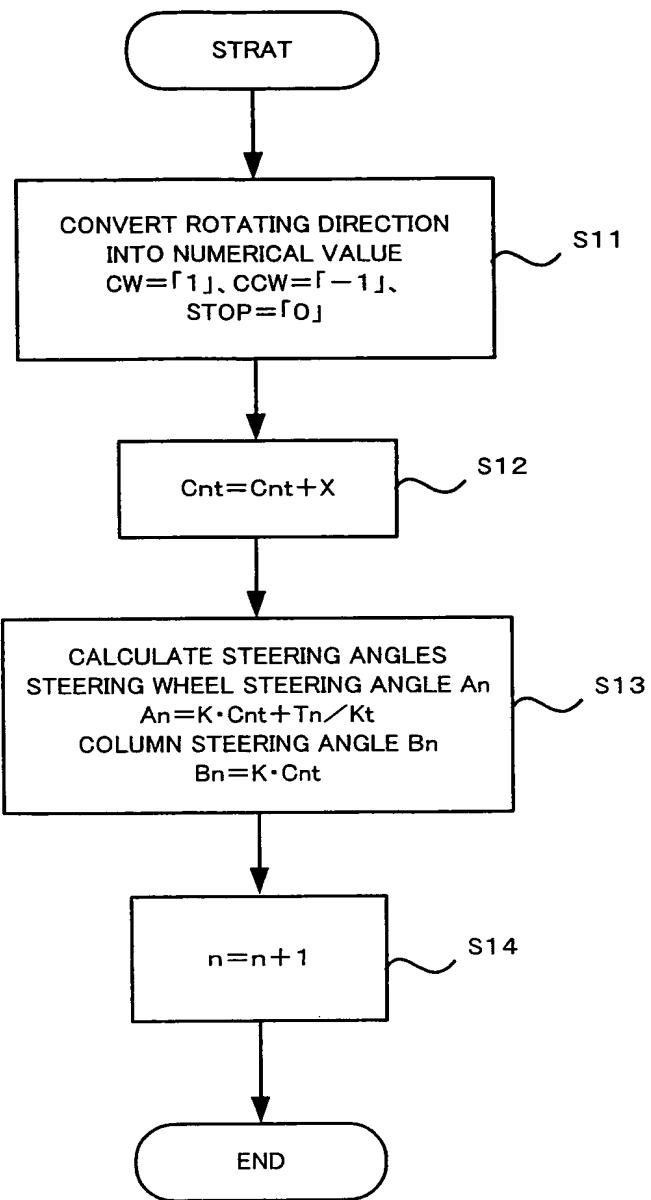
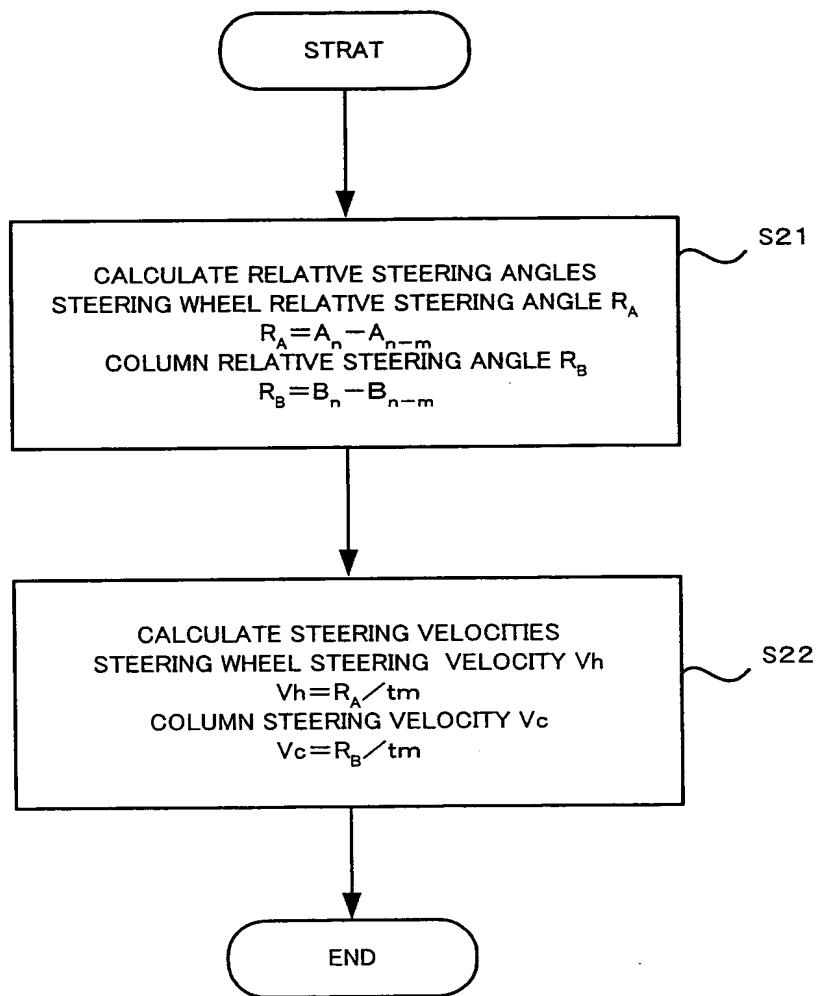


FIG.10



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FIG.11



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